PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

ABB SCHWEIZ AG
Intellectual Property (CH-LC/P)
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SLE-I Eingang 11. JULI 2005 Ablage
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NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(PCT Rule 71.1)

Date of mailing *(day/month/year)*	11.07.2005
Applicant's or agent's file reference 03/014WO	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CH2004/000204	01.04.2004	02.04.2003

Applicant
ABB RESEARCH LTD et al.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary report on patentability and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary report on patentability. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

The applicant's attention is drawn to Article 33(5), which provides that the criteria of novelty, inventive step and industrial applicability described in Article 33(2) to (4) merely serve the purposes of international preliminary examination and that "any Contracting State may apply additional or different criteria for the purposes of deciding whether, in that State, the claimed inventions is patentable or not" (see also Article 27(5)). Such additional criteria may relate, for example, to exemptions from patentability, requirements for enabling disclosure, clarity and support for the claims.

Name and mailing address of the international preliminary examining authority:	Authorized Officer
European Patent Office - Gitschiner Str. 103 D-10958 Berlin Tel. +49 30 25901 - 0 Fax: +49 30 25901 - 840	HALBARTSCHLAGER, M Tel. +49 30 25901-714

PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

Rec'd PCT/PTO 03 OCT 2005
10/551763

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Form PCT/IPEA/416
03/014WO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CH2004/000204	01.04.2004	02.04.2003
International Patent Classification (IPC) or national classification and IPC		
H01L23/24		
Applicant		
ABB RESEARCH LTD et al.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 8 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 3 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
05.11.2004	11.07.2005
Name and mailing address of the international preliminary examining authority:	Authorized Officer
European Patent Office - Gitschiner Str. 103 D-10958 Berlin Tel. +49 30 25901 - 0 Fax: +49 30 25901 - 840	Morena, E Telephone No. +49 30 25901-771

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/CH2004/000204

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages	
1-8	as originally filed
Claims, Numbers	
1-10	filed with telefax on 27.06.2005
Drawings, Sheets	
1/7-7/7	as originally filed

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-10
	No:	Claims	
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-10
Industrial applicability (IA)	Yes:	Claims	1-10
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 In this preliminary report reference is made to the following documents cited in the International Search Report:

D1: EP-A-0962974 (HITACHI LTD) (08-12-1999)
D4: US-B1-6265753 (HEDRICK JAMES L ET AL) (24-07-2001)
D5: US-A-05892289 (TOKUNO KENICHI) (06-04-1999)

2 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of **claims 1-10** does **not** involve an **inventive** step in the sense of Article 33(3) PCT.

2.1 Concerning independent claim 1, document D1 discloses a method for assembling a power semiconductor module, comprising the step of:

- disposing a first electrically conductive layer on at least one portion of a top surface of an electrically insulating substrate, so that at least one peripheral top region of said electrically insulating substrate remains uncovered by the first electrically conductive layer (see figure 1, references 3a and 3b, and column 5, lines 44-46);
- disposing an electrically insulating material on a first corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate (see figure 1, reference 4, and column 4, lines 45-49);
- bonding a semiconductor chip onto said first electrically conductive layer (see column 5, lines 46-53);
- bonding the electrically insulating substrate onto a bottom plate (see column 4, lines 27-31);
- covering said semiconductor chip, said electrically insulating substrate, said first electrically conductive layer, and said first electrically insulating material, at least partially with a second electrically insulating material (see column 4, lines 38-44).

Document D1 further suggest to use polyimide resins as electrically insulating material on said first corner region (see D1, column 7, lines 48-53).
The method of independent claim 1 differs from the teachings of document D1, which is considered to represent the closest prior art document, in the fact that it includes the steps of:

- disposing a small amount of a low viscosity monomer or oligomer precursor of the first electrically insulating material on the first corner region and
- polymerizing it;

and in the fact that:

- the viscosity and the amount of said precursor are chosen so that no air gaps are enclosed between the electrically conductive layer and the peripheral region of said electrically insulating substrate, and
- the surface of the precursor is concave shaped;

Putting into practice the method disclosed by document D1, the man skilled in the at would face the problem of depositing the electrical insulating polyimide resin.
He would recognize in the method described in the document D4 a suitable solution. In fact, document D4 discloses that dielectric material suitable for integrated circuit packages, having enhanced dielectric properties, resistance to cracking and an increased breakdown voltage, can be obtained curing and imidizing a low viscosity solution of an oligomer precursor, comprising a polyamic acid segment (see D4, column 3, line 44 - column 4, line 25). He would also know that low viscosity solutions tend to distribute themselves as a consequence of capillary forces forming concave shaped meniscus, as also shown, for example, by document D5 (see D5, column 5, lines 19-63). He would moreover realize that voids are undesirable because they negatively affect the mechanical and electrical characteristics of the electrically insulating material, and he would consequently try to avoid the occurrence of said voids by adapting the viscosity of the precursor material and/or by suppling it in the appropriate amount.
Finally, it is considered that it would be obvious to the man skilled in the art to combine the teachings of document D4 with the method disclosed by document D1, thus arriving, by the application of known manufacturing principles, to the method as claimed in claim 1 of the present application.

2.2 Dependent claims 2-6 do not contain any additional features which, in combination with the features of the claims to which they refer, meet the criteria of the PCT with respect to

inventive step (Article 33(3) PCT), the reasons being as follows:

a) (claim 2) drop dispense mechanisms are commonly employed in the semiconductor manufacturing industry in order to apply liquid materials, and capillary actions are commonly exploited to distribute them (see for example D5, column 5, lines 19-63);

b) (claim 3) document D1 discloses that the electrically insulating substrate is bonded on a bottom plate before the second electrically insulating material is applied (see D1, figure 1, reference 1 and column 4, lines 27-31);

c) (claim 4) document D1 discloses that at least one second electrically conductive layer is disposed between the bottom plate and at least one portion of a bottom surface of the electrically insulating substrate, so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate (see figure 1); and that a third insulating material is disposed in a second corner formed by the second electrically conductive layer and the peripheral bottom region of the electrically insulating substrate (see figure 10, reference 14, or column 2, lines 24-36). According to the teachings of document D4, depositing a precursor of a third electrically insulating material, instead of the insulating material itself, does not involve an inventive activity;

d) (claim 5) using the same precursor for the third and the first electrically insulating material is a matter of design choice which does not involve an inventive activity;

e) (claim 6) document D1 further discloses that a layer of resin, which is a primer, is provided between the second electrically insulating material and the semiconductor chip, the substrate, the first conductive layer and the first electrically insulating material (see D1 column 6, lines 24-26, and figure 3).

2.3 Referring to independent claim 7, document D1 discloses a power semiconductor module (see D1, column 5, lines 46-50), comprising:

- an electrically insulating substrate (see D1, figure 1, reference 3a, and column 4, line 47);
- a first electrically conductive layer disposed on at least one portion of a top surface of

said electrically insulating substrate, so as to selectively expose at least one peripheral top region of said electrically insulating substrate (see D1, figure 1, reference 3b; column 4, lines 47-48, or column 5, lines 44-46)

- at least one semiconductor power chip bonded on said electrically conductive layer (see D1, column 5, lines 46-50);

- an electrically insulating substrate is bonded on a bottom plate (see D1, column 4, lines 27-31);

- a first electrically insulating material disposed in a corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate (see D1, figure 1, reference 4 or figure 10, reference 14);

- a second insulating material at least partially embedding said semiconductor power chip, said electrically insulating substrate, said first electrically conductive layer, and said first electrically insulating material (see D1, figure 1, reference 5a, or figure 10, reference 5b);

whereby the first electrically insulating material is a polyimide (see D1, column 7, lines 48-53). The power semiconductor module of independent claim 7 differs from the disclosure of document D1, which is considered to represent the closest prior art document, only in the fact that the surface of the first electrically insulating material is concave-shaped. However, this feature is considered a mere consequence of the method adopted to form the insulating material, and it appears that it does not solve any technical problem and has no specific technical effect. Consequently, the subject-matter of claim 7 is considered to be not inventive over the disclosure of document D1 (Article 33(3) PCT).

2.4 Dependent claims 8-10 do not contain any additional features which, in combination with the features of claim 7 to which they refer, meet the criteria of the PCT with respect to inventive step. In fact, document D1 further discloses that:

a) (claim 8) the electrically insulating substrate is mounted on a bottom plate (see D1, figure 1, reference 1 and column 4, lines 27-31);

b) (claim 9) at least one second electrically conductive layer is disposed between the bottom plate and at least one portion of a bottom surface of the electrically insulating substrate, so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate (see figure 1); and a third insulating material is disposed in a second corner formed by the second electrically conductive layer and the peripheral

bottom region of the electrically insulating substrate (see figure 10, reference 14, or column 2, lines 24-36).

c) (claim 10) a "rigid" layer of resin is provided between the second electrically insulating material and the semiconductor chip, the substrate, the first conductive layer and the first electrically insulating material (see figure 3 references 5a and 5b, and column 6, lines 24-26).

3 All the **claims 1-10** are considered as **industrially applicable** and therefore meet the criteria of Article 33(4) PCT.

Re Item VIII
Certain observations on the international application

1 The terms "low viscosity" used in claim 1, and "rigid", used in claim 10, are vague and unclear and leave the reader in doubt as to the meaning of the technical features to which they refer, thereby rendering the definition of the subject-matter of said claims unclear (Article 6 PCT).

PATENT CLAIMS

ART 34 AMDT

1 A method for assembling a power semiconductor module, comprising the steps of:

- disposing a first electrically conductive layer (4) on at least one portion of a top surface of an electrically insulating substrate (2), so that at least one peripheral top region of said electrically insulating substrate (2) remains uncovered by the first electrically conductive layer (4);
- disposing a precursor (51) of a first electrically insulating material (5) in a first corner region (24) formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2);
- polymerizing the precursor (51) of the first electrically insulating material (5) to form the first electrically insulating material (5);
- bonding a semiconductor chip (6) onto said first electrically conductive layer (4);
- bonding the electrically insulating substrate (2) onto a bottom plate (11);
- covering said semiconductor chip (6), said electrically insulating substrate (2), said first electrically conductive layer (4), and said first electrically insulating material (5) at least partially with a second electrically insulating material (8);

characterized in that

- the precursor (51) of the first electrically insulating material (5) is a low viscosity monomer or oligomer that forms a polyimide when polymerizing, and in that
- small amounts of said precursor (51) are being applied to the junction of said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2), so that no air gaps are enclosed between the electrically conductive layer (4) and the electrically insulating substrate (2), and in that
- the precursor is distributed along said junction, and in that
- the surface of the precursor (51) disposed in the corner region formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2) is formed concave-shaped.

2 The method as claimed in claim 1, characterized in that drop dispense mechanism is used for applying drops of the precursor (51) to the junction of said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2)), and that the precursor distributes itself along said junction by capillary forces.

ART 34 AMDT

3 The method as claimed in claim 1, characterized in that the electrically insulating substrate (2) is bonded onto a bottom plate (11) before the second electrically insulating material (8) is applied.

4 The method as claimed in one of the previous claims, further comprising the steps of

- disposing at least one second electrically conductive layer (3) between the bottom plate (11) and at least one portion of a bottom surface of the electrically insulating substrate (2), so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate (2); and
- disposing a precursor of a third electrically insulating material in a second corner (23) formed by the second electrically conductive layer (3) and the peripheral bottom region of the electrically insulating substrate (2).

5 The method as claimed in one of the previous claims, characterized in that the precursor of the third electrically insulating material is identical to the precursor of the first electrically insulating material.

6 The method as claimed in one of the previous claims, characterized in that a primer is disposed to at least partially cover the semiconductor chip (6), the electrically insulating substrate (2), the first electrically conductive layer (4), and the first electrically insulating material (5) before the second insulating material is attached.

7 A power semiconductor module, comprising:

- an electrically insulating substrate (2);
- a first electrically conductive layer (4) disposed on at least one portion of a top surface of said electrically insulating substrate (2), so as to selectively expose at least one peripheral top region of said electrically insulating substrate (2);
- at least one semiconductor power chip bonded on said electrically conductive layer (4);
- an electrically insulating substrate (2) is bonded on a bottom plate (11);
- a first electrically insulating material (5) disposed in a corner region formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2);

- a second insulating material (8) at least partially embedding said semiconductor power chip, said electrically insulating substrate (2), said first electrically conductive layer (4), and said first electrically insulating material (5);

characterized in that

- the first electrically insulating material (5) is a polyimide, and
- the surface of the first electrically insulating material (5) disposed in the corner region formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2) is concave-shaped.

8 The power semiconductor module as claimed in claim 7, characterized in that the electrically insulating substrate (2) is mounted on a bottom plate (11).

9 The power semiconductor module as claimed in claim 7 or 8, characterized in that at least one second electrically conductive layer (3) is disposed between the bottom plate (11) and at least one portion of a bottom surface of the electrically insulating substrate (2), so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate (2); and that a third insulating material (9) is disposed in a second corner (23) formed by the second electrically conductive layer (3) and the peripheral bottom region of the electrically insulating substrate (2).

10 The power semiconductor module as claimed in claim 7, 8 or 9, characterized in that a rigid layer (7) of resin is provided between the second electrically insulating material (8) and the semiconductor chip (6), the substrate (2), the first conductive layer (4) and the first electrically insulating material (5).

AMENDED CLAIMS

REPLACED BY ART 34 AMDT

[Received by the International Bureau on 20 August 2004 (20.08.04): original claims on pages 9 and 10 replaced by amended claims on pages 9 and 10]

1 A method for assembling a power semiconductor module, comprising the steps of:

- disposing a first electrically conductive layer (4) on at least one portion of a top surface of an electrically insulating substrate (2), so that at least one peripheral top region of said electrically insulating substrate (2) remains uncovered by the first electrically conductive layer (4);
- disposing a precursor (51) of a first electrically insulating material (5) in a first corner region (24) formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2);
- polymerizing the precursor (51) of the first electrically insulating material (5) to form the first electrically insulating material (5);
- bonding a semiconductor chip (6) onto said first electrically conductive layer (4);
- bonding the electrically insulating substrate (2) onto a bottom plate (11);
- covering said semiconductor chip (6), said electrically insulating substrate (2), said first electrically conductive layer (4), and said first electrically insulating material (5) at least partially with a second electrically insulating material (8);

characterized in that

- the precursor (51) of the first electrically insulating material (5) is a low viscosity monomer or oligomer that forms a polyimide when polymerizing, that
- small amounts of said precursor (51) are being applied to the junction of said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2), whereas
- the amount of said precursor is so small that no air gaps are enclosed between the electrically conductive layer (4) and the electrically insulating substrate (2), and that
- the precursor is distributed along said junction, and that
- the surface of the precursor (51) disposed in the corner region formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2) is formed concave-shaped.

2 The method as claimed in claim 1, characterized in that drop dispense mechanism is used for applying drops of the precursor (51) to the junction of said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2)), and that the precursor distributes itself along said junction by capillary forces.

3 The method as claimed in claim 1, characterized in that the electrically insulating substrate (2) is bonded onto a bottom plate (11) before the second electrically insulating material (8) is applied.

4 The method as claimed in one of the previous claims, further comprising the steps of

- disposing at least one second electrically conductive layer (3) between the bottom plate (11) and at least one portion of a bottom surface of the electrically insulating substrate (2), so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate (2); and
- disposing a precursor of a third electrically insulating material in a second corner (23) formed by the second electrically conductive layer (3) and the peripheral bottom region of the electrically insulating substrate (2).

5 The method as claimed in one of the previous claims, characterized in that the precursor of the third electrically insulating material is identical to the precursor of the first electrically insulating material.

6 The method as claimed in one of the previous claims, characterized in that a primer is disposed to at least partially cover the semiconductor chip (6), the electrically insulating substrate (2), the first electrically conductive layer (4), and the first electrically insulating material (5) before the second insulating material is attached.

7 A power semiconductor module, comprising:

- an electrically insulating substrate (2);
- a first electrically conductive layer (4) disposed on at least one portion of a top surface of said electrically insulating substrate (2), so as to selectively expose at least one peripheral top region of said electrically insulating substrate (2);
- at least one semiconductor power chip bonded on said electrically conductive layer (4);
- an electrically insulating substrate (2) is bonded on a bottom plate (11);
- a first electrically insulating material (5) disposed in a corner region formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2);